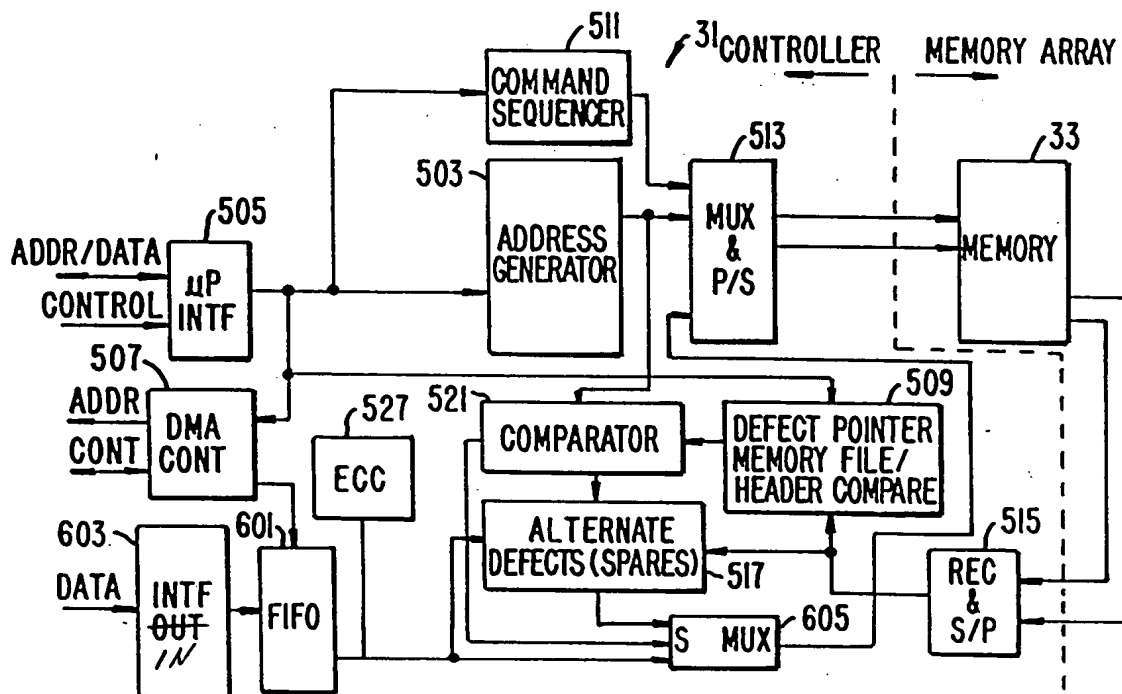


The diagram illustrates a memory system architecture. At the top, a **CONTROLLER** (511) is connected to a **MEMORY ARRAY** (33). The controller sends signals to a **COMMAND SEQUENCER** (511) and an **ADDRESS GENERATOR** (503). The **ADDRESS GENERATOR** (503) outputs to a **MUX & P/S** (513), which then connects to the **MEMORY** (33). A **DATA** path (505) flows from the **MEMORY** (33) through an **INTF OUT** (525) and a **FIFO** (519) to an **INTF** (505). The **INTF** (505) is also connected to a **DMA CONT** (507) and a **COMPARATOR** (521). The **DMA CONT** (507) receives **ADDR/CONTROL** (507) and **DATA** (525) inputs. The **COMPARATOR** (521) is connected to an **ECC** (527) and an **ALTERNATE DEFECTS (SPARES)** (523) block. The **ALTERNATE DEFECTS (SPARES)** (523) block is connected to a **MUX** (523) and a **RECT & S/P** (515) block. The **RECT & S/P** (515) block is connected to the **MEMORY** (33) and the **CONTROLLER** (511). A **DEFECT POINTER MEMORY FILE/HEADER COMPARE** (509) block is also connected to the **CONTROLLER** (511) and the **COMPARATOR** (521).



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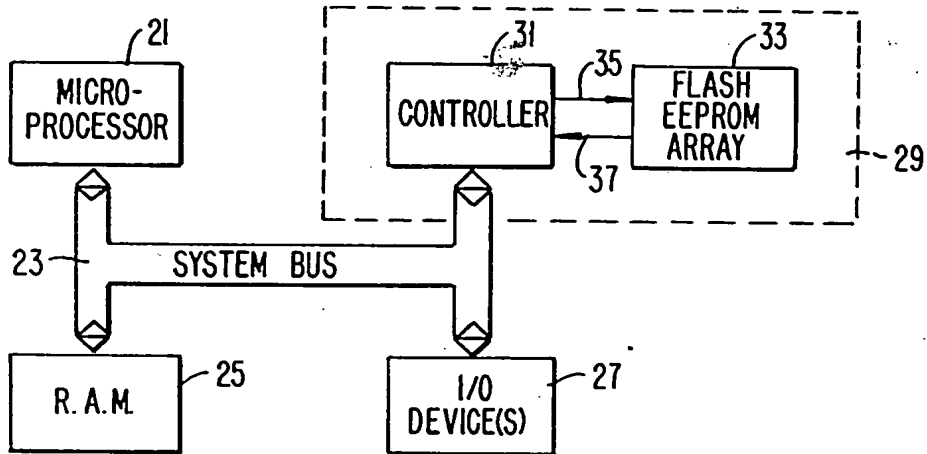


FIG. 1A.

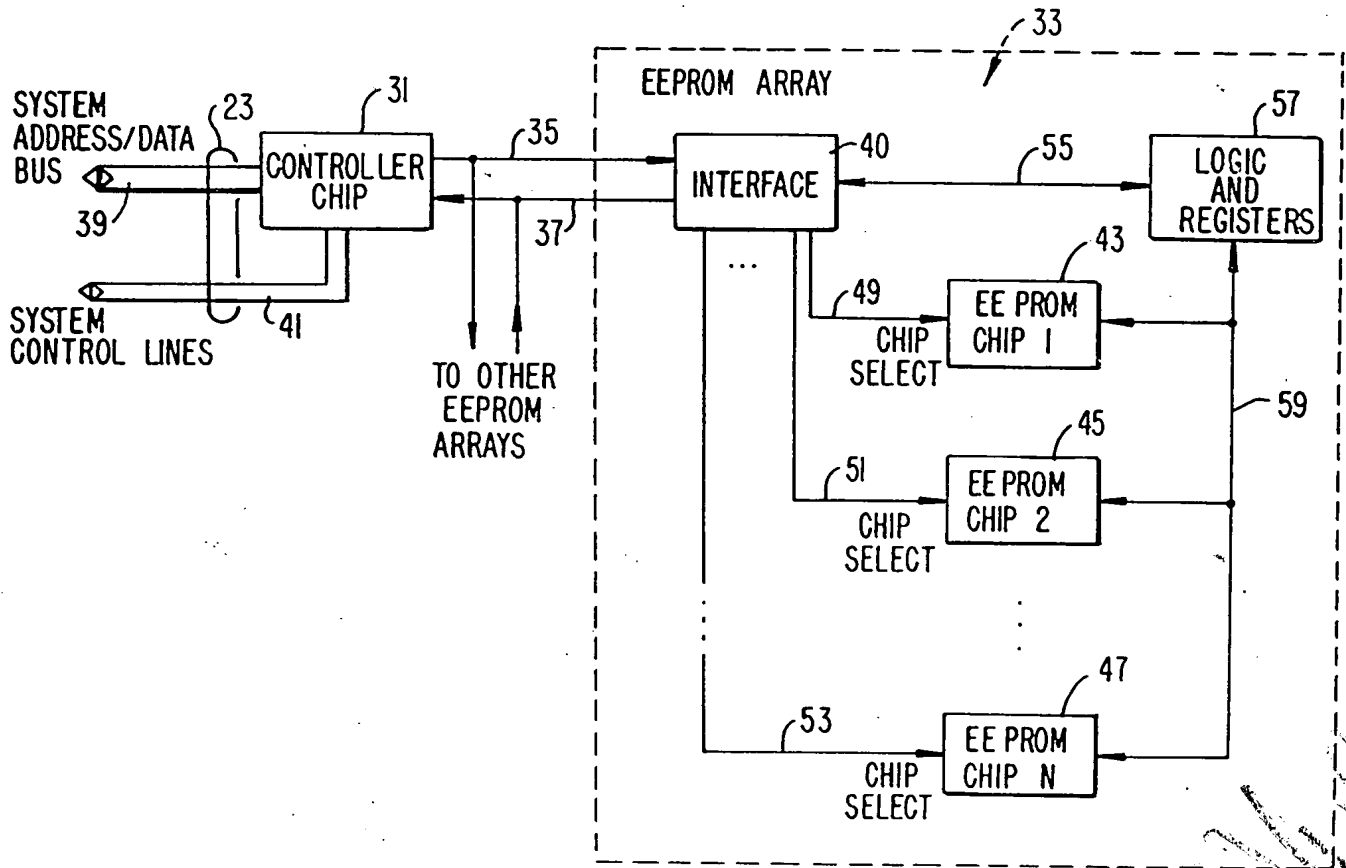


FIG. 1B.

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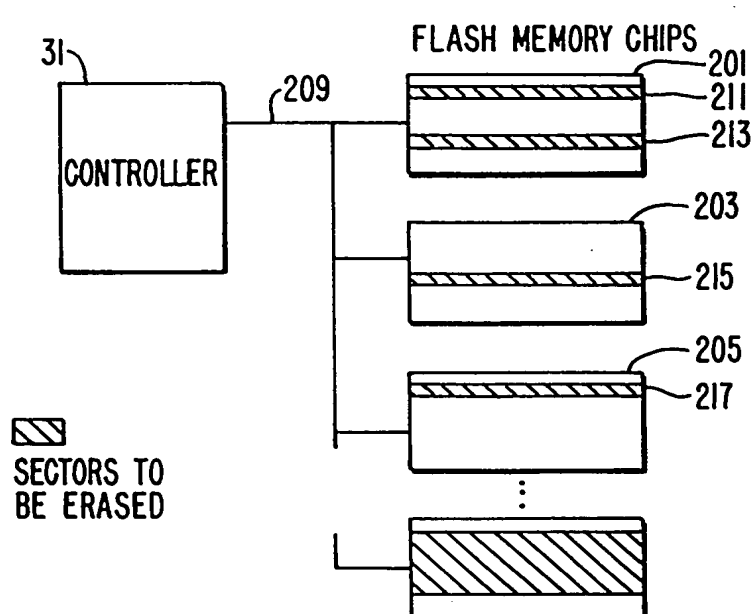


FIG. 2.

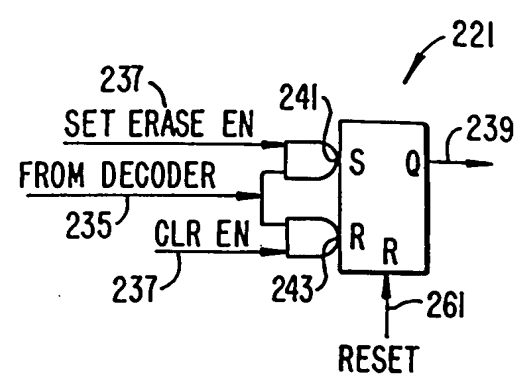


FIG. 3B.

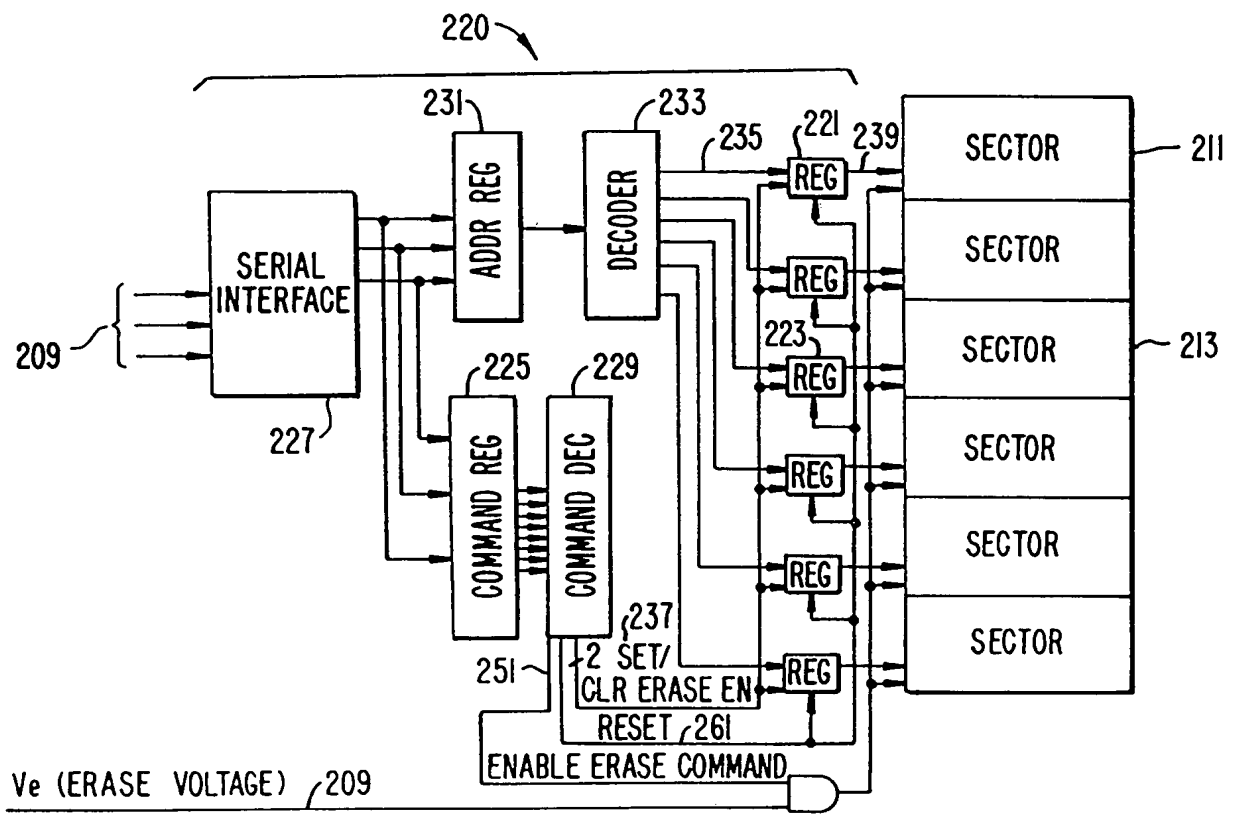


FIG. 3A.

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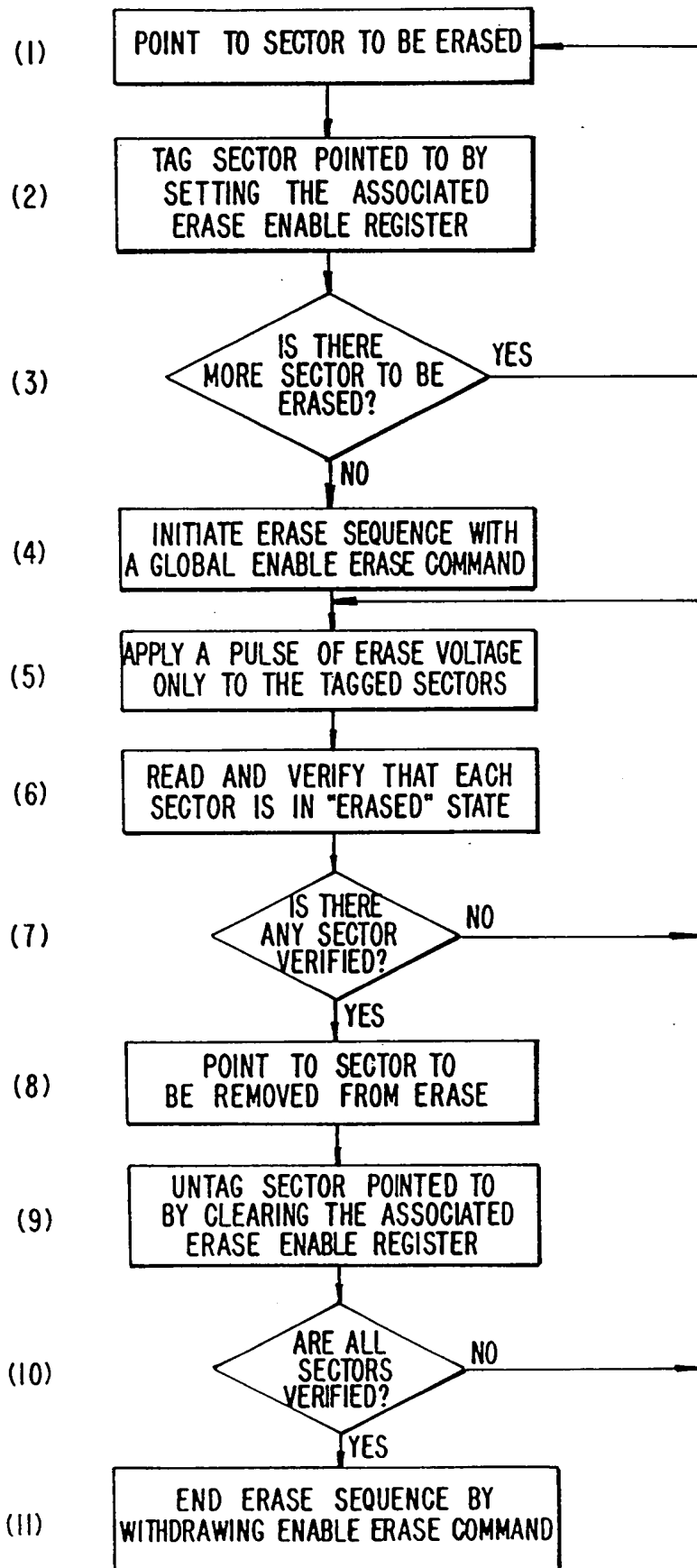
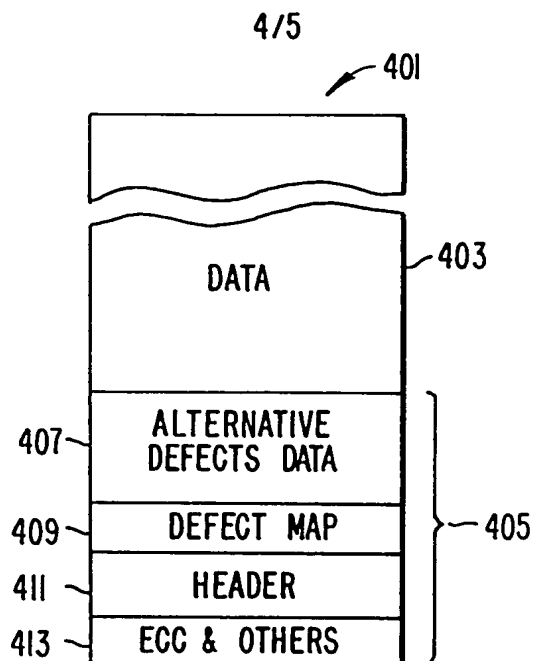


FIG. 4.

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SECTOR PARTITION
FIG. 5.

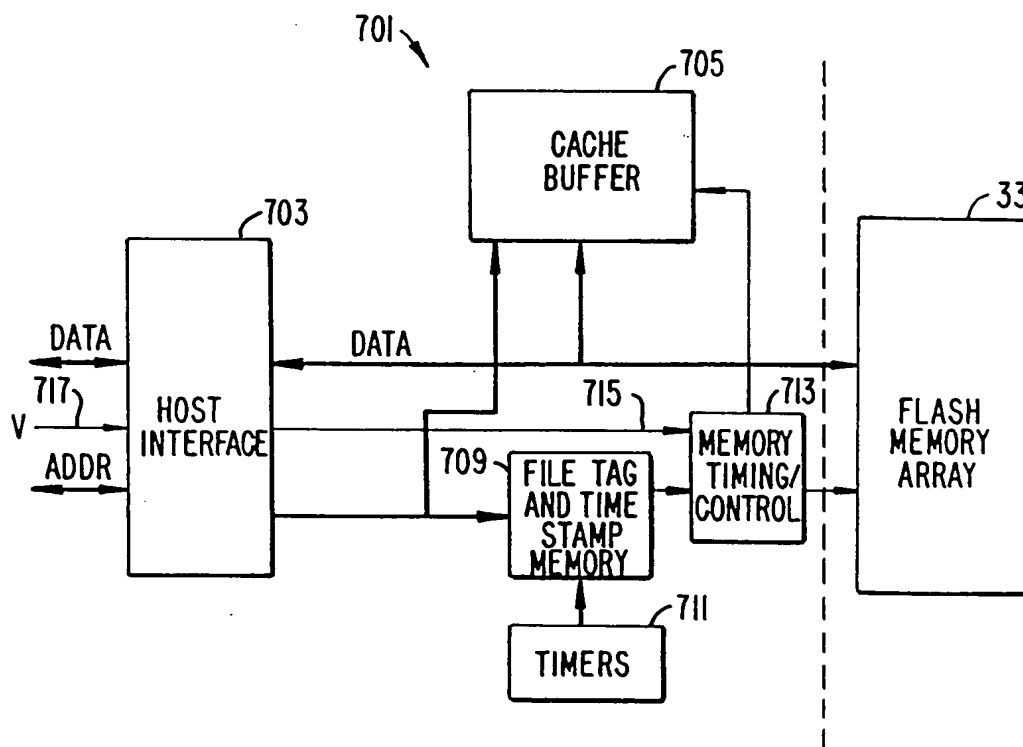
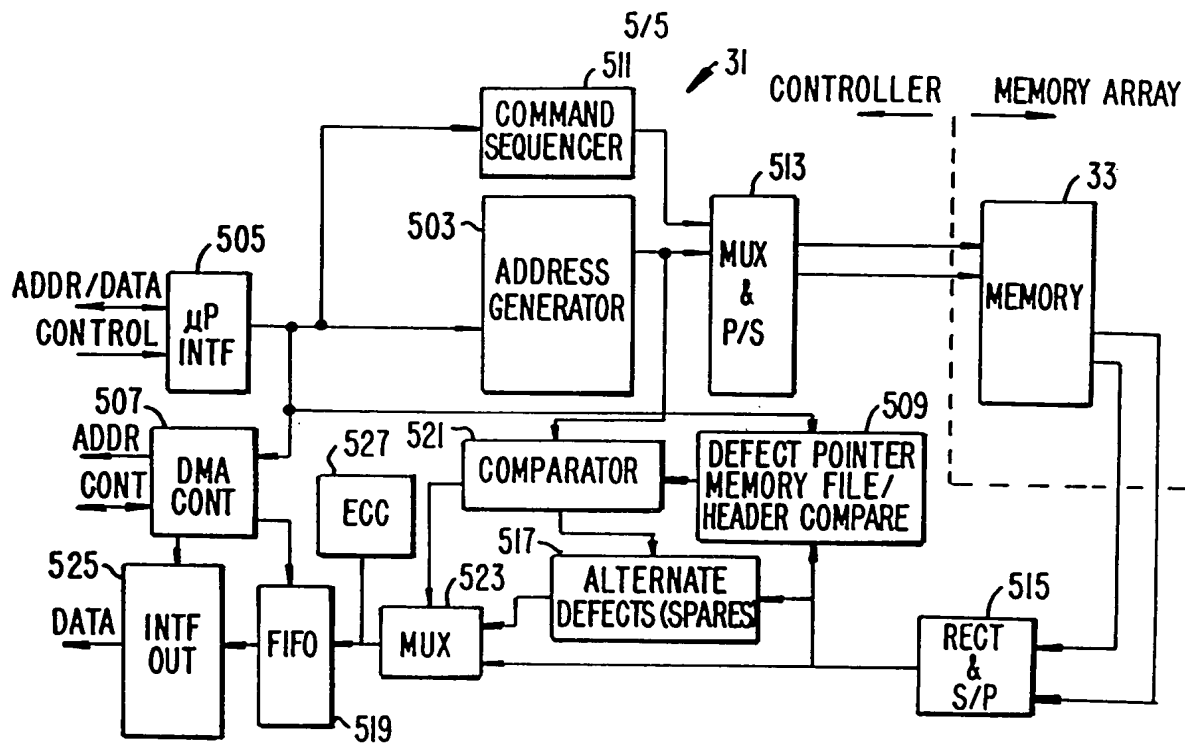


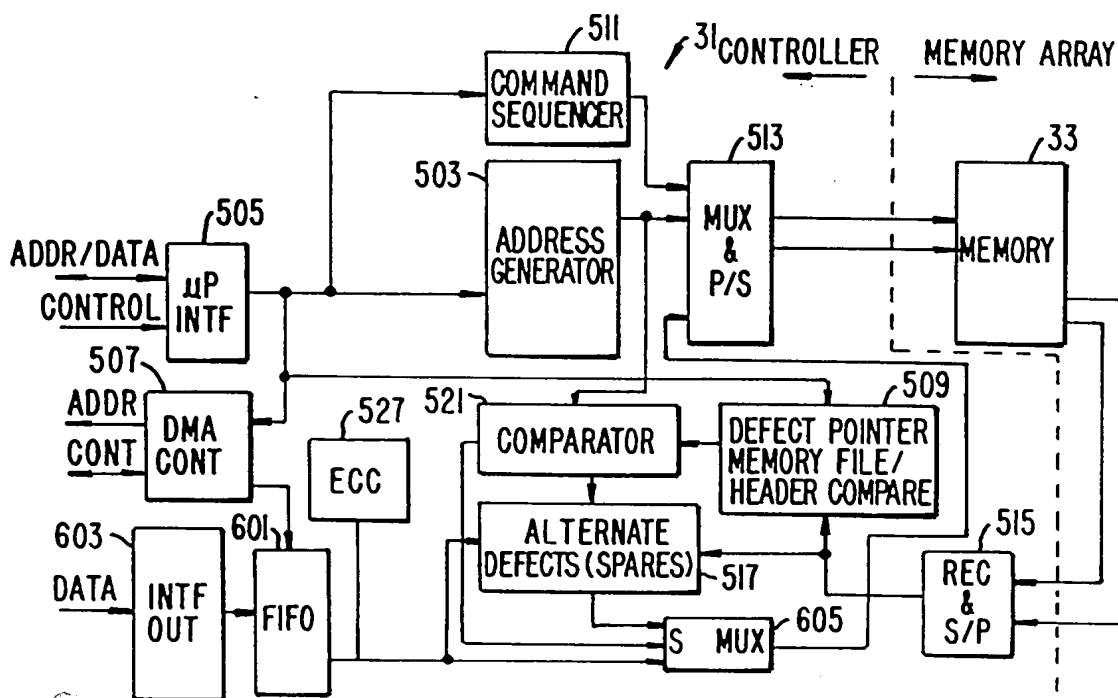
FIG. 8.

0899498-122997



READ DATA PATH CONTROL

FIG. 6.



WRITE DATA PATH CONTROL

FIG. 7.

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"8646680"